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DEVELOPMENT OF PULSED PROCESSES FOR THE MANUFACTURE OF SOLAR CELLS

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"THE JPL LOW-COST SILICON SOLAR ARRAY PROJECT IS SPONSORED BY THE U.S. DEPARTMENT OF ENERGY AND FORMS PART OF THE SOLAR PHOTOVOLTAIC CONVERSION PROGRAM TO INITIATE A MAJOR EFFORT TOWARD THE DEVELOPMENT OF LOW-COST SOLAR ARRAYS. THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY BY AGREEMENT BETWEEN NASA AND DOE."

PREPARED UNDER CONTRACT NO. 954785 FOR:

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DEVELOPMENT OF PULSED PROCESSES FOR THE MANUFACTURE OF SOLAR CELLS

Contract Number 954786

For the Period of
15 September - 15 December 1978

Prepared for:
JET PROPULSION LABORATORY
California Institute of Technology
Pasadena, CA 91103

Prepared by: _____
Principal Investigator

Approved by: _____
Program Manager

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ABSTRACT

This report describes the first quarter results under the continuation of a program to develop ion implantation, pulse processes, and the equipment for the automated production of silicon solar cells. The report describes the development status of the process based upon ion implantation for the introduction of junctions and back surface fields. A process sequence is presented employing ion implantation and pulse processing. Efforts to improve throughput and decrease process element costs for furnace annealing are described. Design studies for a modular 3,000 wafer per hour pulse processor are discussed.

TABLE OF CONTENTS

Section			Page
1	INTRODUCTION		1-1
2	PROCESS DEVELOPMENT		2-1
	2.1	Ion Implantation Parameters	2-1
	2.2	Process Sequence Development	2-3
	2.3	Furnace Annealing	2-7
	2.4	Pulsed Electron Beam Annealing	2-12
		2.4.1 Development of 7.6-cm Diameter Electron Beams	2-12
		2.4.2 Step and Repeat Pulse Annealing for 20 x 20 cm Areas	2-16
		2.4.3 Solid Phase Epitaxial Regrowth Annealing	2-20
3	MANUFACTURING FEASIBILITY		3-1
	3.1	Pulsed Electron Beam Machine Design	3-1
		3.1.1 Power Supplies for Pulsed Electron Beam Processors	3-7
		3.1.2 Pulse Forming Network	3-9
		3.1.3 High Voltage Switching	3-9
	3.2	Scanning DC Electron Beam Annealing	3-10
	3.3	Belt Furnace Hardware	3-14
4	SUMMARY		4-1
5	RECOMMENDATIONS		5-1
6	NEW TECHNOLOGY		6-1
7	PROGRAM SCHEDULE		7-1
	REFERENCES		R-1

LIST OF FIGURES

Figure		Page
2-1	Relative Ion Beam Current on Wafer From Freeman Ion Source With BF_3 Gas Feed	2-5
2-2a	Fluorine Atomic Profiles Obtained from SIMS Measurements on (100) Si Implanted at Room Temperature With a $1x10^{15}$ $-cm^{-2}$ Fluence of BF_2^+	2-6
2-2b	Net Acceptor Concentration Profile Obtained From a High-Fluence BF_2 Implant and 550°C Isothermal Anneal	2-6
2-3	Furnace Cycles Selected for Cost Performance Optimization for Ion Implantation Annealing	2-8
2-4	Sheet Resistance Across 5-cm Diameter Implant Anneal by Pulsed Electron Beam	2-13
2-5	Photographs of 7.6-cm (3-inch) and 5.0-cm (2-inch) Electron Beam Anneal Signature on Phosphorus Implanted Wafers	2-14
2-6	Sheet Resistance Across 7.6-cm Diameter Implant Anneal by Pulsed Electron Beam	2-15
2-7	Schematic of Mask Experiments for Processing Discrete Anneal Areas Within Implanted Wafers	2-17
2-8	Schematic Representation of Mask Edge Details for Pulsed Electron Beam Processing	2-18
2-9a	Microphoto of Edge of Anneal Pattern Using Carbon Mask 0.5 mm (0.02 inch) Off Wafer, Showing Uniformly Sharp Contour Change	2-19
2-9b	Square Pattern Anneal (1 Pulse) Covering One-Quarter of Sample	2-19
2-10	Photograph of Step and Repeat Anneal Pattern on 4x4 cm Ion-Implanted Silicon Sheet	2-20
3-1	Summary of Existing Experience on the Use of Pulsed Energy Annealing of Ion Implantation Damage	3-3
3-2	Electron Beam Energy Spectrum for SPI-PULSE 600 Pulsed Electron Beams	3-4
3-3	Typical Pulsed Electron Beam Anneal Signature for Overlap Pulses for Step and Repeat Operation of SPI-PULSE 600	3-6
3-4	Schematic for 125 cm^2/sec Belt Furnace for Implant Annealing	3-15
7-1	Program Schedule	7-2

LIST OF TABLES

Table		Page
2-1	Furnace Anneal Test Matrix for Solar Cell Implant Annealing	2-7
2-2	Process Sequence for Ion-Implanted n+/pp+, High-Efficiency Solar Cells	2-10
2-3	Summary of Solar Cell Performance for Furnace Anneal Test Matrix	2-11
3-1	Comparative Specifications and Costs for Power Supplies for Pulse Processor Applications	3-8
3-2	Functional Requirements for 250 cm^2/sec Belt Furnace for Implant Annealing	3-15

SECTION 1
INTRODUCTION

This is the first quarterly report under phase II of contract 954786, which is being performed for the JPL-LSA project to develop ion implantation, pulse processes, and process equipment. Development over the long term is directed towards an extremely abbreviated process sequence for the manufacture of solar cells. This process sequence does not include any thermal heat treatments or wet chemistry. The emphasis of the second phase of the contract is upon pulse process development and demonstration of the technology.

Under a previous contract[1], it was demonstrated that silicon solar cells can be fabricated very rapidly without furnace treatments, wet chemistry, or gas atmosphere operations if ion implantation is employed in conjunction with pulse annealing. The deliverable solar cells were 2 x 2 cm demonstration devices with efficiencies up to 12.3 percent AM1. Under phase I of this contract[2], ion-implanted, pulse annealed cells were delivered with efficiencies up to 15 percent AM1, and implanted, furnace annealed cells were delivered with an average efficiency of 15 percent AM1 and peak efficiencies greater than 16.5 percent AM1 for 7.6-cm (3-inch) diameter solar cells.

Efforts in pulse processing are now concentrated on establishing the pulsed electron beam parameters necessary to anneal 7.6-cm (3-inch) diameter solar cells with a single pulse. Demonstration of this technology is to be accomplished by delivery of five hundred 7.6-cm diameter solar cells with ion-implanted, pulsed electron beam annealed junctions and back surface fields.

SECTION 2
PROCESS DEVELOPMENT

2.1 ION IMPLANTATION PARAMETERS

The ion implantation parameters for this development effort are identical to those optimized for furnace annealing under phase I of this contract. These parameters were developed within the constraints of state-of-the-art implanter hardware able to produce boron and phosphorus ion beams in the 1 to 4 mA and 10 to 50 keV ranges.

The following two types of implants in 10-ohm-cm Czochralski silicon were adopted, to develop the required electron beam parameters for pulse annealing wafers 7.6 cm in diameter with a single pulse:

Junction: n+ layer
2×10^{15} cm^{-2} $^{31}P+$, 10 keV, 10° incidence
Implant at 0.1 mA/cm^2 current density

Back Surface Field: p+ layer
5×10^{15} cm^{-2} $^{11}B+$, 25 keV, 10° incidence
Implant at 0.05 mA/cm^2 current density

Both phosphorus and boron ions are implanted with a Varian/Extrion 200-1000 WF machine with a dose uniformity of $\pm$10 percent across the 7.6 cm wafer surface and dose reproducibility of $\pm$1 percent from wafer to wafer.

Additional process development effort is being expended on making the existing furnace anneal procedures more cost effective by decreasing the time required at elevated temperatures. The implant parameters for this anneal optimization matrix are also identical to those specified above.

Upon completion of the pulse anneal and furnace anneal steps just described, a new set of implant parameters will be investigated for both junction and back surface field (BSF) implantation. Ions for the new investigation will include $^{27}Al+$ for back surface fields and $^{75}As+$ for junction implants.

If the requirements for mass-analyzed ion beams can be relaxed for solar cell manufacturing, implantation equipment for back surface field p^+ layers can be greatly simplified, with reduced capital equipment costs the result. Examples of such simplified equipment (if the process sequence can be modified and successfully demonstrated) include:

1. Liquid metal ion sources -- Charged particles are produced with high beam currents of aluminum, gallium, and other metals. Sources with 2.5 mA beam currents are now commercially available for gallium. The source provides 0.1 - 10.0 keV ions from a jet of liquid metal directed into a plasma.

2. Hollow cathode ion sources — Without mass analysis these sources, originally developed for ion thrusters, can deliver ampere-level beams over a large area. Typical current densities are 3 mA/cm^2 at 1 - 2 keV. By controlling the purity of the ion source material, nonintentional ion species can be controlled. This method of implantation, although not mass-analyzed, will be usable for effective p^+ layers, provided the implant anneal is done properly as discussed below.

3. Biased electron beam evaporator — This type of system has sometimes been referred to as low-energy ion implantation; however, the system is essentially an electron beam heated evaporator with an ionization field around the melt region and a voltage of 10-20 kV applied between the melt and the substrates to be coated. The effect is to provide improved adhesion of the evaporant to the substrates.

For each of the above three methods of implanting aluminum, boron, or gallium ions, the purity specifications of the ion beams can be relaxed significantly if pulse heating is used to anneal the implantation damage and to activate the implanted ions. The ion source purity requirements are lessened for pulse annealing because spurious dopants contained within the aluminum source material when implanted cannot diffuse more rapidly than the aluminum during transient heating and rapid quenching. In contrast, furnace annealing requires long times (typically 15 - 30 minutes) at an elevated temperature, allowing fast diffusing impurities to migrate to the bulk silicon. For example, titanium, a common impurity found in most aluminum material, has a diffusion

coefficient larger than aluminum. The effect of spurious contaminants, which include magnesium and iron, as well as titanium, on solar cell performance is a net reduction of carrier lifetimes, diffusion lengths, and solar cell current.

The method of introducing the p^+ layer also influences the selection of the pulse anneal energy source. If the aluminum layer, for example, is to be introduced by ion implantation, either pulsed electron beams or pulsed lasers can be used for annealing. However, if charged particles are used for thick-film aluminum deposition, then the electron beam method must be used, since lasers with 1-micrometer wavelengths cannot effectively couple the beam energy because of optical reflection.

2.2 PROCESS SEQUENCE DEVELOPMENT

Many advantages can be realized for large-scale manufacturing by using low-temperature, vacuum processing in place of high-temperature, furnace processing. Examples include:

1. Absence of oxidizing atmosphere and subsequent oxide etches, waste treatment for oxide etches, and wet-chemistry operations.
2. Compatibility with automation requirements such as process control and in-line processing on inexpensive cell carriers.
3. Higher efficiency cells probably achievable. (Nearly perfect lattice regrowth occurs during liquid phase epitaxial pulse annealing. During ion implantation and pulse annealing the bulk silicon is never brought to high temperatures, thereby precluding lifetime degradation by thermally induced defects.)
4. Pulse processing based on ion implantation and pulse annealing possibly advantageous for fabricating cells using advanced polycrystalline sheet materials. (Transient, surface heating will minimize effects such as diffusion of dopants and contact metallization along grain boundaries and other defects.)
5. Integration of implant and pulse annealing accomplishable quite easily with a common vacuum chamber for both processes.

The above advantages, in addition to the characteristics of line-of-sight ion beam and electron beam processing, eliminate the need for edge treatments for junction and BSF

isolation. The following process sequence has been selected:

1.	Etch	Texturize, flash, or plasma assisted
2.	Implant BSF p+	$5x10^{15}$ $^{11}B+$ or $^{27}Al+$ cm^{-2} at 10 keV (+ 10% dose tolerance) at 3-4 mA/cm^2 current density. Mass analysis may not be required for BSF aluminum processing.
3.	Pulse anneal BSF	0.2 cal/cm^2, 10 keV, 100 ns pulsed electron beam, liquid phase epitaxy mode.
4.	Implant junction n+	$2x10^{15}$ $^{21}P+$ cm^{-2} at 10 keV (+10% dose tolerance) at 3-4 mA/cm^2 current density.
5.	Pulse anneal junction	0.2 cal/cm^2, 10 keV, 100 ns pulsed electron beam, liquid phase epitaxy mode.
6.	Deposit back contact	400A Al plus base metal for conductance. Method to be determined.
7.	Deposit front contact grid	400A Ta, Mo, W, or Pd written by charged particle or ink jet technology.
8.	AR coat	Plasma assisted Si_3N_4 chemical vapor deposition

A few of the process steps listed above require proof of feasibility for solar cell production. These steps include a method for additive contact printing such as charged particle writing and ink jet writing (step 7). The BSF-implant parameters also require optimization for pulse anneal processing (step 2), including the parameters for the ion species, $^{11}B+$ and $^{27}Al+$, as well as the molecular implants, $^{49}BF_2+$ and AlH_x+. The advantage of molecular implants is the higher available beam currents from Freeman-type ion sources. For example, Figure 2-1 shows the mass-analyzed ion beam spectrum for BF_3 gas in a hot-filament, Freeman-type ion source. Approximately 40 percent more ion beam current and, therefore, greater throughput is available for $^{49}BF_2+$ than for $^{11}B+$ ions. Pulse annealing $^{49}BF_2+$ implants (step 3) has yet to be investigated for activating boron ions as a BSF, while diminishing the effects caused by retention of the fluorine atoms in the silicon lattice. By comparison, furnace annealing has been found to be inadequate for activating BF_2 for the following two reasons: (1) High current implants of $^{11}B+$ or $^{49}BF_2+$ at room temperature do not produce a totally amorphous region, and therefore such implanted boron atoms become difficult to activate electrically with furnace techniques[3] (see Figure 2-2a); and (2) retention of fluorine is evident in the thermal annealing of $^{49}BF_2+$ implants[3] (see Figure 2-2b).

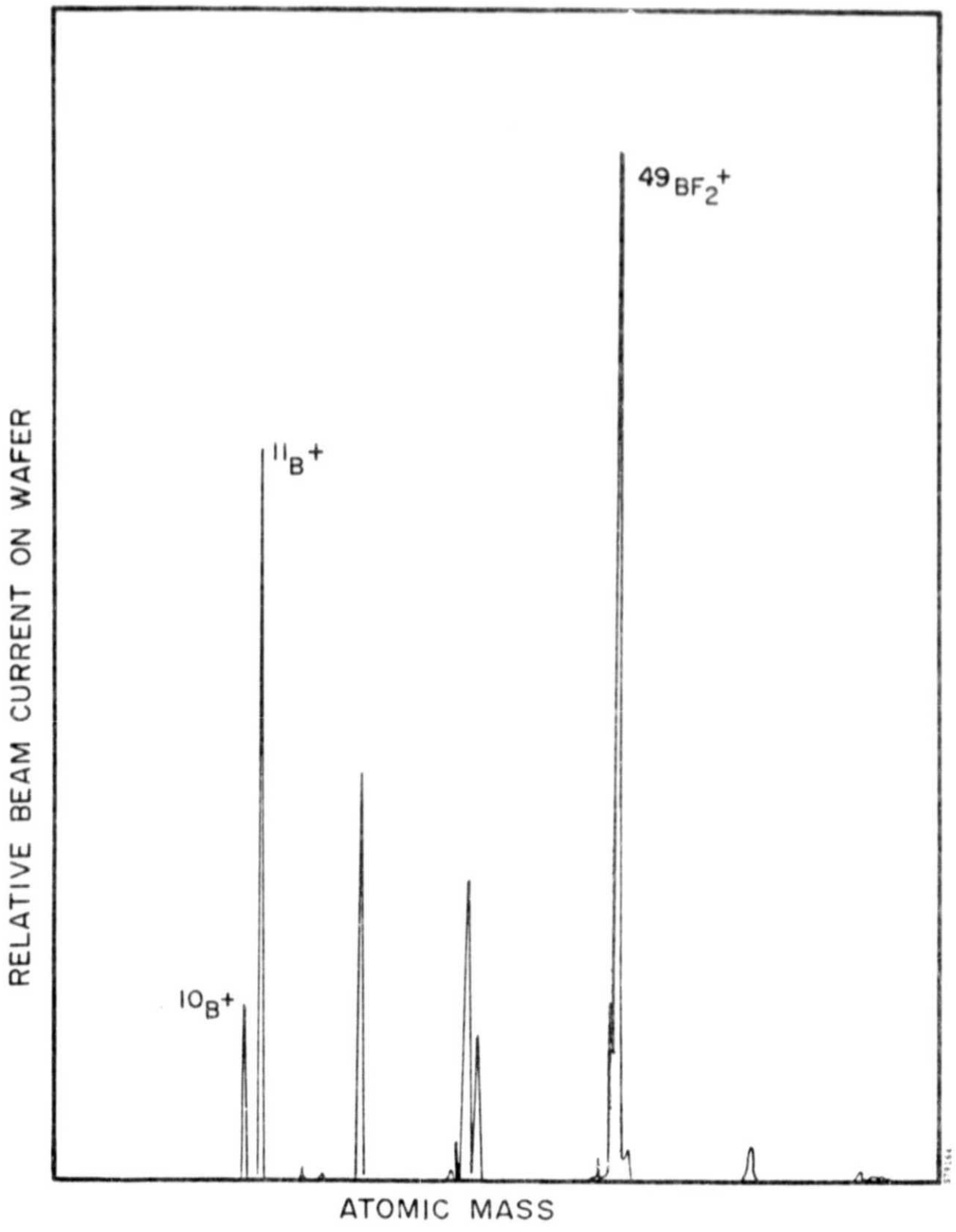


FIGURE 2-1. RELATIVE ION BEAM CURRENT ON WAFER FROM FREEMAN ION SOURCE WITH BF_3 GAS FEED

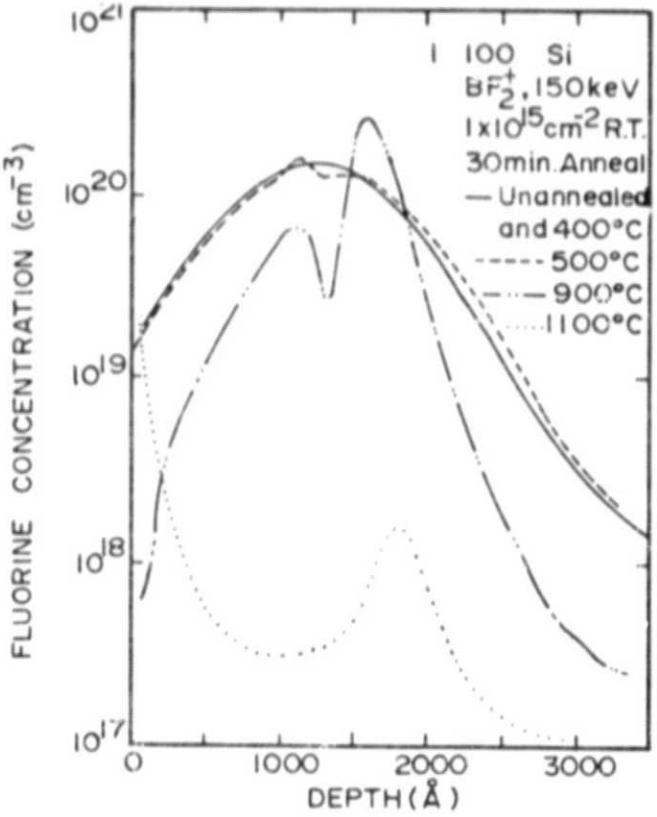


FIGURE 2-2a. FLUORINE ATOMIC PROFILES OBTAINED FROM SIMS MEASUREMENTS ON (100) Si IMPLANTED AT ROOM TEMPERATURE WITH A $1x10^{15}$ $-cm^{-2}$ FLUENCE OF BF_2^+ (See Ref. 3.)

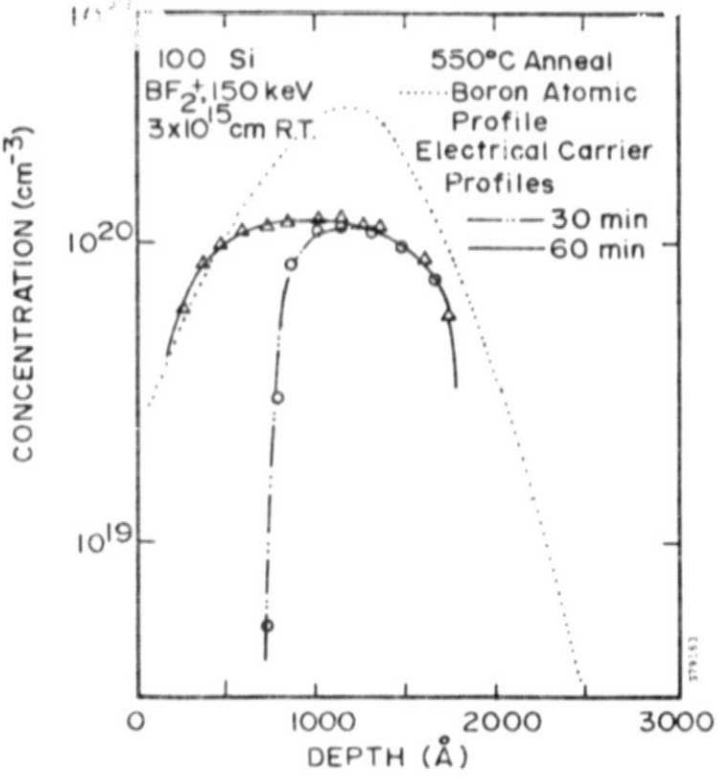


FIGURE 2-2b. NET ACCEPTOR CONCENTRATION PROFILE OBTAINED FROM A HIGH-FLUENCE BF_2^+ IMPLANT AND 550°C ISOTHERMAL ANNEAL (See Ref. 3.)

2.3 FURNACE ANNEALING

One key element in manufacturing high-efficiency solar cells with back surface fields in Czochralski silicon is the annealing of ion implantation lattice damage. Performance-optimized annealing procedures were developed under phase I of this contract for simultaneous n+ junction and p+ BSF annealing in a standard tube furnace. However, these procedures were not optimized with respect to cost effectiveness, but rather for demonstrating high-efficiency solar cell manufacturing by ion implantation. For example, cells with efficiencies as high as 16.5 percent (AM1-28°C) were produced using the very long anneal schedule described below.

The objective of the present effort, under phase II of the contract, is to reduce the process time at temperature while maintaining cell efficiency. For reference, the performance-optimized anneal process element was specified and verified by other contractors as follows:

2 hours	-	550°C
15 minutes	-	850°C
2 hours	-	550°C

A furnace temperature program was not used, so that all heating and cooling was rapid and typical of the manual transfer of quartz wafer holders into and out of a tube furnace.

A furnace anneal matrix was designed and utilized for processing solar cell lots of 20 wafers each. The test matrix for furnace anneal optimization is shown in Table 2-1 and Figure 2-3.

TABLE 2-1. FURNACE ANNEAL TEST MATRIX FOR SOLAR CELL IMPLANT ANNEALING

Cycle	Time at Temperature (minutes) 550°C	850°C	550°C
Baseline	120	15	120
1	—	15	120
2	—	15	60
3	—	15	—
4	60 ramp	15 ramp	60
5	— belt furnace —		
6	60	15	—
7	60	15	60

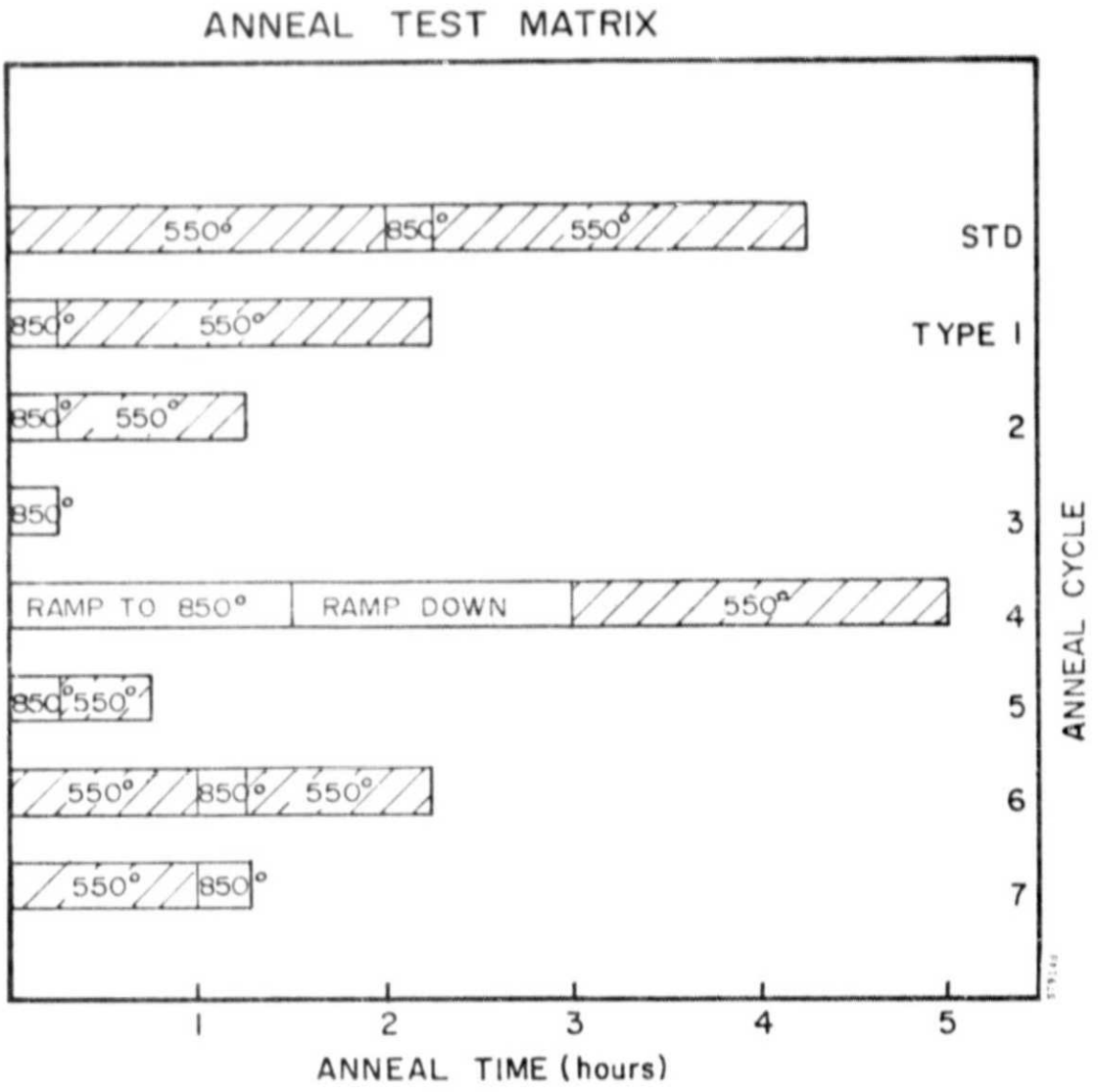


FIGURE 2-3. FURNACE CYCLES SELECTED FOR COST-PERFORMANCE OPTIMIZATION FOR ION IMPLANTATION ANNEALING
(Note: All temperatures shown are ^{o}C)

Cycle 4 in Table 2-1 refers to temperature-programmed heating and cooling rates; the cycle is defined as follows:

1. 550°C - 1 hour (solid phase epitaxial regrowth)
2. Heated at 13.6°C/min to 850°C
3. 850°C - 15 min (activation of implanted species to substitutional lattice sites)
4. Cool at 3.3°C/min to 550°C
5. 550°C - 1 hour (lifetime enhancement)

Cycle 5 in Table 2-1 refers to a commercial belt or tunnel furnace commonly used for metal sintering processes with a hydrogen atmosphere. Belt furnaces can be designed and fabricated for large production rates with tantalum chambers and chain drives to minimize contamination by nonintentional dopants. Further discussion of the feasibility and economics of belt furnace annealing is included in Section 3.

The starting silicon material for this furnace anneal test matrix was characterized as follows:

Specification	Range
Resistivity:	10 ohm-cm and 1 ohm-cm ±25%
Diameter:	7.62 cm
Thickness:	300 micrometers ±10%
Orientation:	(100)
Surfaces:	Etched to remove saw damage
Growth:	Czochralski
Type:	p-Boron doped

All the material was processed as shown in Table 2-2. Both 1 and 10 ohm-cm silicon was evaluated with the baseline anneal cycle, to determine the sensitivity of this implanted-furnace anneal process sequence to doping levels in the as-grown silicon material. The results of the anneal matrix are shown in Table 2-3 for both 1- and

TABLE 2-2. PROCESS SEQUENCE FOR ION-IMPLANTED, n+/pp+, HIGH-EFFICIENCY SOLAR CELLS

Silicon Material	10-ohm-cm, (100), CZ, p-type, 300 micrometers thick, flash etched
Process Sequence	
Implant:	Junction - 2×10^{15} $^{31}P^+$ cm^{-2}, 10 keV, 10° Back surface field - 5×10^{15} $^{11}B^+$ cm^{-2}, 25 keV, 10°
Implant Uniformity:	No worse than ±10 percent across wafer Approximately ± 1 percent wafer to wafer
Anneal:	Simultaneous phosphorus and boron implant anneal in nitrogen (see Table 2-1 for process specifications)
Clean:	Buffered HF Deionized water rinse
Front Metallization:	Evaporate 400A Ti + 400A Pd + 1,000A Ag Define Spire Starburst pattern with standard Kodak KTFR process Electroplate 12 micrometers of Ag
Clean:	Buffered HF Deionized water rinse
Back Metallization:	Evaporate 400A Ti + 400A Pd + 1 micrometer of Ag
AR Coating:	Evaporate 700A TiO_2
Sinter:	400°C - 10 minutes in nitrogen
Test:	AM1 I-V and spectral response

TABLE 2-3. SUMMARY OF SOLAR CELL PERFORMANCE FOR FURNACE ANNEAL TEST MATRIX

Anneal Cycle	AM0-25°C Characteristics				Resistivity (ohm-cm)
	I_{sc} (amperes)	V_{oc} (volts)	P_{max} (watts)	Fill Factor	
Baseline	1.760 (0.026)	0.587 (0.001)	0.77 (0.03)	0.74 (0.02)	10
Baseline	1.628 (0.048)	0.596 (0.006)	0.70 (0.04)	0.72 (0.03)	1.0
1	1.753 (0.022)	0.585 (0.002)	0.76 (0.02)	0.74 (0.01)	10
2	1.744 (0.024)	0.586 (0.002)	0.77 (0.01)	0.75 (0.01)	10
3	1.703 (0.140)	0.579 (0.005)	0.68 (0.13)	0.69 (0.10)	10
4	1.710 (0.043)	0.567 (0.001)	0.70 (0.09)	0.72 (0.08)	
5	*	*	*	*	10
6	*	*	*	*	10
7	*	*	*	*	10

Note: The standard deviation is shown in parentheses after each mean value.

* Indicates that data is not yet complete.

10-ohm-cm Czochralski silicon. These experiments have shown that significant time can be saved in furnace anneal process requirements with little performance loss. Specifically, the Type 2 anneal, which consists of 15 minutes at 800°C followed by 60 minutes at 550°C, is as effective as the 255-minute baseline process. The results also show that higher cell efficiencies are obtainable with 10-ohm-cm silicon than with 1-ohm-cm when processed with ion-implanted junctions and BSF's. Better efficiencies are achieved because of the higher short-circuit currents resultant from longer carrier lifetime in the more lightly doped silicon, while the BSF increases open-circuit voltage of cells processed with 10-ohm-cm material to 600 mV.

2.4 PULSED ELECTRON BEAM ANNEALING

2.4.1 Development of 7.6-cm Diameter Electron Beams

Pulsed electron beams are being developed which can be used to anneal ion implantation damage in a 7.6-cm diameter wafer with a single pulse. Results over the entire surface of the wafer must be at least as good as the pulse anneal results with the previous 5.0-cm diameter beam, as shown in Figures 2-4 and 2-5. This requires a macroscopic uniformity (fluence averaged over 1 cm^2) of ± 5 percent and a microscopic uniformity (variations with characteristic dimensions less than 1 mm) better than ± 10 percent. The surface of the sample must be annealed with no region damaged and with no region of high resistivity for all length scales.

Beam propagation experiments were designed with parameters extrapolated from the 5-cm diameter beam. All length scales were increased by 50 percent and the energy stored in the pulse forming network was increased by a factor of 2.25 to anneal the larger area. After a suitable geometry was found, the results were as shown in Figure 2-6. The electron beam is focused from an initial diameter of 10 cm at the cathode to a diameter of 7.6 cm at the sample, using a steady, magnetic axial field of about 1 kilogauss for electron beam uniformity control. Some optimization to improve solar cell electrical performance is still required to improve the open-circuit voltage of completed devices.

During the large-diameter beam experiments, the high-voltage design limits on the pulse generator were exceeded, damaging the pulse forming network, power supply, and magnet. Further work was delayed while the facility was upgraded. Specifically, a new power supply was built, the transmission line was replaced with a better quality one, and a new magnet was constructed with a water-cooled core. Experiments with a 7.6-cm diameter beam have been resumed.

As part of this task, the following simplified electron beam generator cathode-anode diode geometries were tested and discarded. In one test setup the implanted silicon wafer was used as an anode directly without the conventional anode grid. The beam was filamentary and resulted in damage to the silicon material. A sufficient drift distance must be provided for self-interaction between electrons to scatter nonuniform beam structures created at the cathode, while the cathode-anode gap cannot be changed and is less than the required drift distance. Another

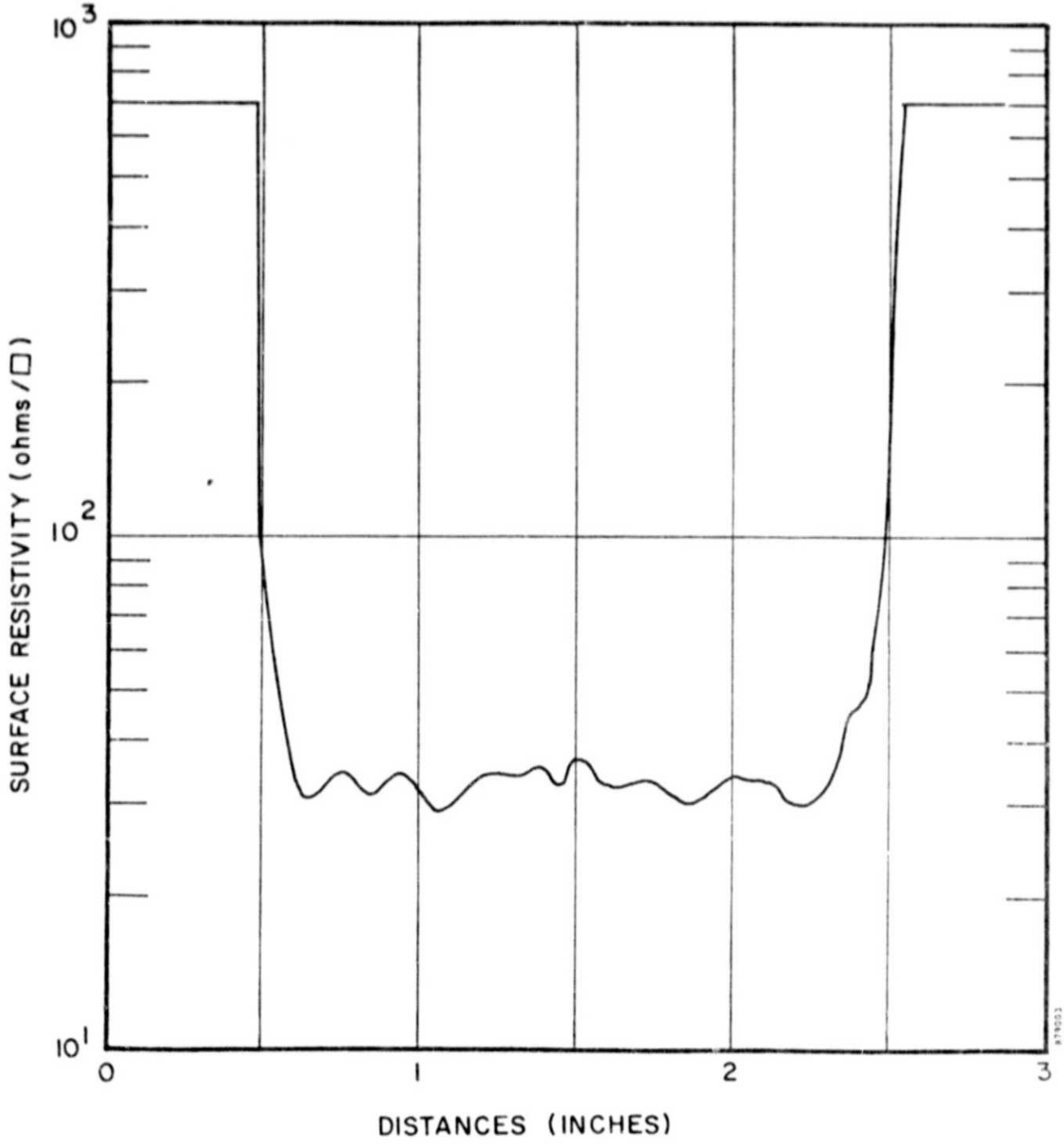


FIGURE 2-4. SHEET RESISTANCE ACROSS 5-cm DIAMETER IMPLANT ANNEAL BY PULSED ELECTRON BEAM

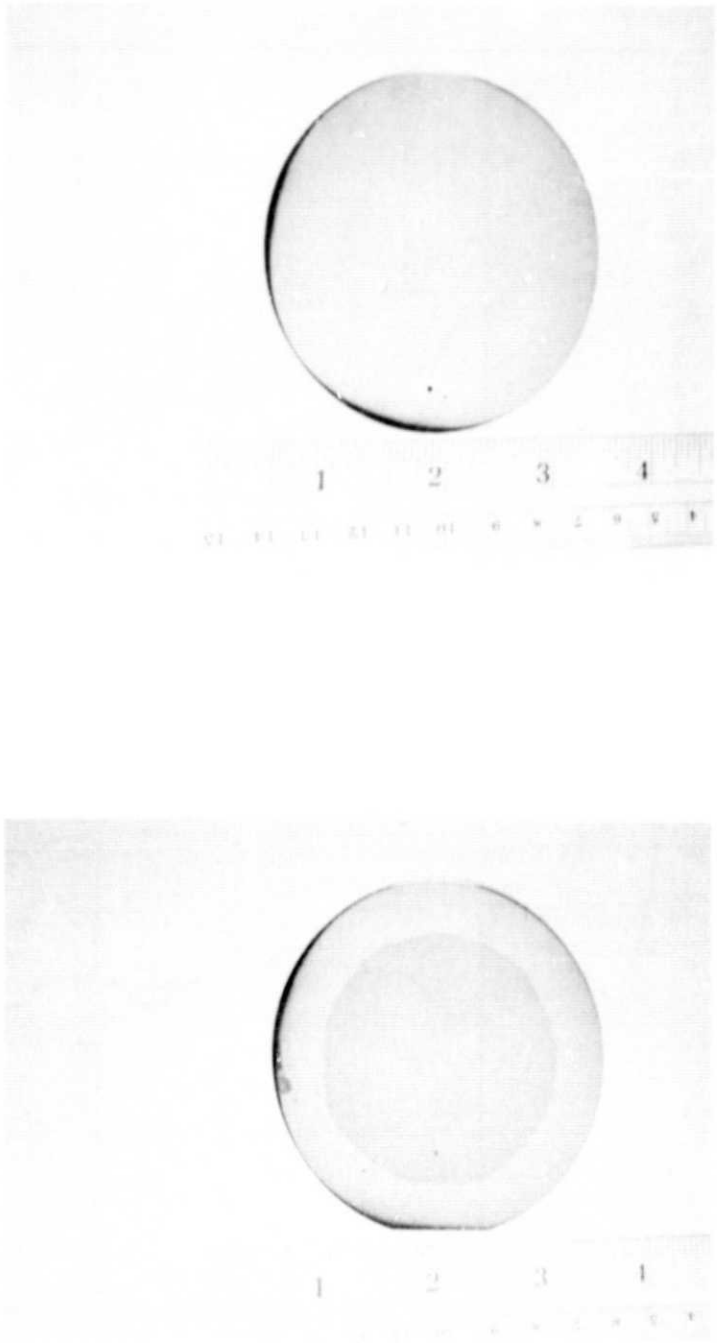


FIGURE 2-5. PHOTOGRAPHS OF 7.6-cm (3-INCH) AND 5.0-cm (2-INCH) ELECTRON BEAM ANNEAL SIGNATURE ON PHOSPHORUS IMPLANTED WAFERS

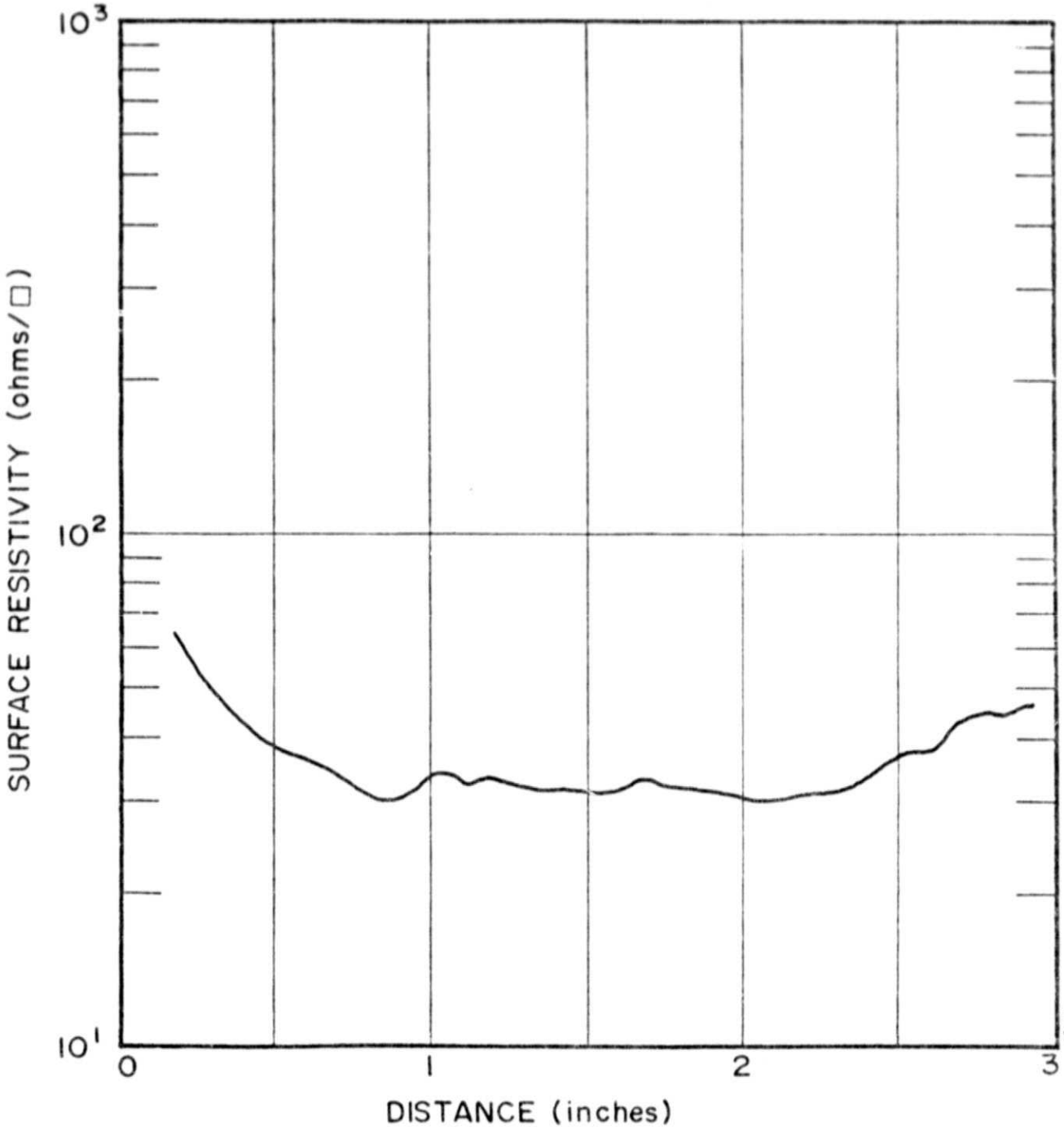


FIGURE 2-6. SHEET RESISTANCE ACROSS 7.6-cm DIAMETER IMPLANT ANNEAL BY PULSED ELECTRON BEAM

test configuration considered propagation of a 7.6-cm beam with an equal size cathode. The diameter of a 7.6-cm electron beam from a 7.6-cm cathode was not maintained at the required current density. A low density background gas could, when ionized, neutralize the self-fields of the beam, but the gas would create excessive contamination in the form of ions accompanying the electron beam pulse.

2.4.2 Step and Repeat Pulse Annealing for 20 x 20 cm Areas

Separate electron beam pulses which anneal ion implantation damage in silicon can be overlapped leaving the region at the intersection annealed and undamaged. A pattern with a maximum dimension less than 3.8 cm was replicated over a 7.6-cm diameter implanted wafer, sufficient for a solar cell demonstrating that the technique will work on larger areas.

There are two approaches to large-area annealing with a circular electron beam pattern. The simpler method is to move the sample material beneath the beam in such a manner that eventually the entire area is in the beam. The disadvantage of this technique is that 40 percent of the surface is pulsed two or three times (with a square packing pattern), so that excessive diffusion of the implanted dopant in this multiply heated region may adversely affect the solar cell output. The alternative approach, chosen for this study, is to create a noncircular beam (i.e., square) by the use of a mask which can define an area for annealing with minimal overlap and dopant diffusion. Because the beam is focused and contains a very high current, a pattern generated at the cathode will not propagate to the silicon sample in a uniform corresponding pattern.

The experimental configuration was as shown in Figure 2-7. The beam mask was fashioned from a high-density graphite sheet 0.5 mm thick. This material shows high resistance to damage from melting or spalling from pulsed, high-power electron beams and has negligible x-ray yield (i.e., it is suitable for production line machines). The mask was held in place and grounded through electrically conductive grease to the sample holder. Figure 2-8 shows various details of the edge configuration for the mask. With the mask touching the sample, a thin crack in the wafer at the carbon-silicon-vacuum interface always developed, independent of the geometry shown in Figure 2-8. The damage is believed to result from a vacuum problem, since with the mask in contact with or close to the wafer the region between the two is not effectively

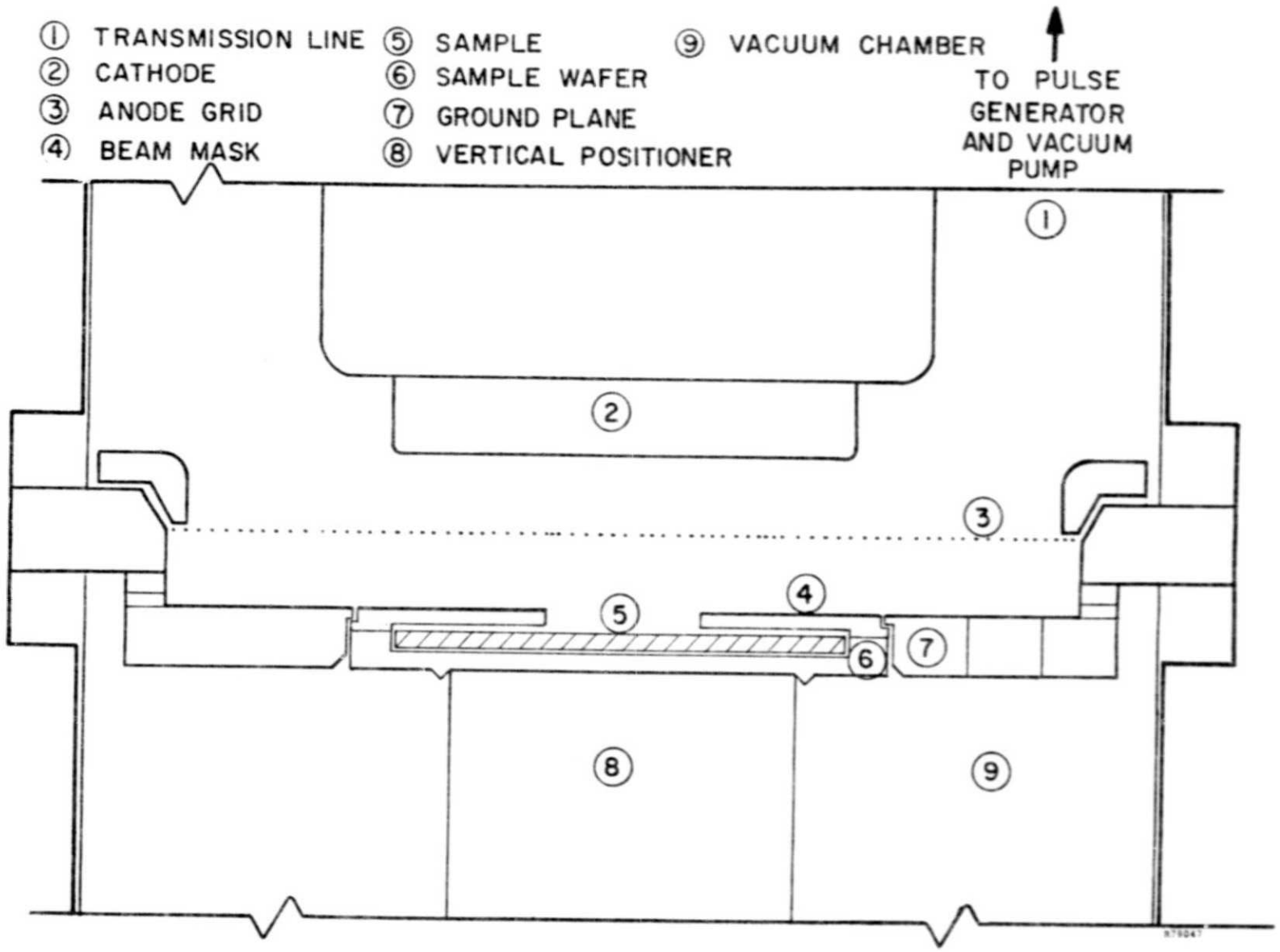


FIGURE 2-7. SCHEMATIC OF MASK EXPERIMENTS FOR PROCESSING DISCRETE ANNEAL AREAS WITHIN IMPLANTED WAFERS

pumped. With a slight enhancement of pressure (due to the grease), the electron beam arcs to the interface point. When the mask was raised off the surface by about 0.5 mm (see Figure 2-8), the damage was prevented. Irregularities in the edge of the annealed pattern on the implanted wafer, as shown in Figure 2-9, were less than 0.5 mm, and inside this edge the anneal was uniform. The pattern can be replicated, as shown in Figure 2-10, without cracking the sample.

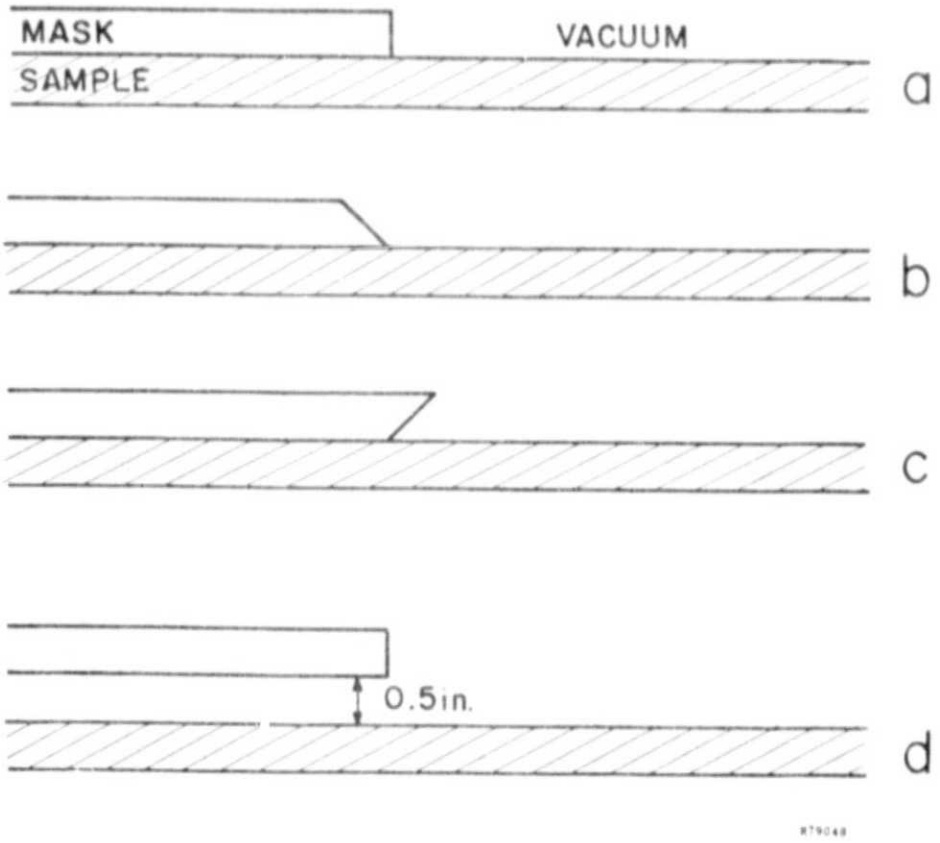


FIGURE 2-8. SCHEMATIC REPRESENTATION OF MASK EDGE DETAILS FOR PULSED ELECTRON BEAM PROCESSING



FIGURE 2-9a. MICROPHOTO OF EDGE OF ANNEAL PATTERN USING CARBON MASK 0.5 mm (0.02 inch) OFF WAFER SHOWING UNIFORMLY SHARP CONTOUR CHANGE

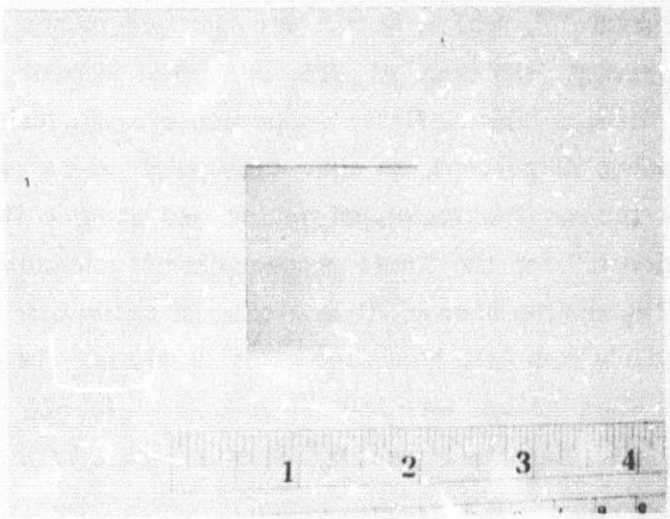


FIGURE 2-9b. SQUARE PATTERN ANNEAL (1 PULSE) COVERING ONE-QUARTER OF SAMPLE

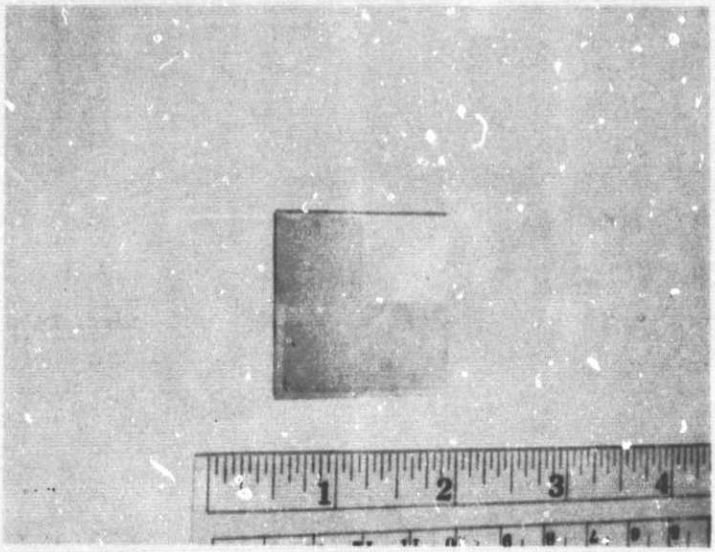


FIGURE 2-10. PHOTOGRAPH OF STEP AND REPEAT ANNEAL PATTERN ON 4 x 4 cm ION-IMPLANTED SILICON SHEET

2.4.3 Solid Phase Epitaxial Regrowth Annealing

An alternative approach to annealing large-area sheet materials is to develop a lower temperature pulse annealing technique, based upon solid phase epitaxial regrowth of the crystal structure[3], which would use multiple pulses at lower fluence. This technique would prevent diffusion of the implanted dopant and allow the use of overlapping beams without masks. Here, the percentage of overlap from one pulse to the next is high, exceeding 90 percent, so that each point on the silicon surface would be pulsed 10 or more times. The technique was tested using a fluence of 0.6 joule/cm^2, compared to 1 joule/cm^2 for the liquid phase epitaxial annealing normally used, for 10 successive shots. The sample showed little electrical activation of the implanted dopant after 1 pulse but nearly complete annealing after 10 pulses. The point probe open-circuit voltage under AM0 illumination was 480 mV compared to 520 mV from a single pulse anneal and 540 mV after furnace annealing. Results would improve with optimization of the technique.

SECTION 3
MANUFACTURING FEASIBILITY

3.1 PULSED ELECTRON BEAM MACHINE DESIGN

Significant changes in the electron beam generator are required to build a pulse processor for annealing 600 cm^2/sec of ion-implanted silicon. At 50 cm^2/pulse for annealing, this processor would trigger at $4x10^8$ times per year. Currently, the existing facility at 50 cm^2/pulse requires maintenance every $1-2x10^3$ pulses. The lifetime of the production facility between maintenance downtime is a key requirement. The goal of this effort was to identify the technology for the power supply, energy store and pulse forming networks, switch, and beam cathode-anode components capable of meeting the functional requirements for beam fluence, pulse width, pulse repetition rate, and lifetime between periods of scheduled maintenance.

Once it is given that a single large pulse is no longer suitable (i.e., a beam 20 x 20 cm square is not considered feasible because of the extremely high currents that must be switched) and given that step and repeat annealing is a realistic process to consider, the energy of a single pulse is variable. The fluence, or energy per unit area, must remain constant, but the diameter of the electron beam can vary. The economic balance between a smaller number of high-energy electron beam geneators and many smaller, but simpler beam generators is being determined but is outside the scope of this effort. Here, we note the technical benefits of using smaller, lower energy beams:

- The lifetime of a high-current switch increases as the energy per pulse decreases.
- The transmission lines, or replacement components, will have a greater lifetime and smaller size. Volume scales roughly as the square of the energy in a pulse.
- The anode may not be needed, focusing may not be required, contamination can be reduced, and the mask (described in Section 2.4.2) may not be necessary.

The assumption of approximately constant fluence is based upon fixed material properties and a narrow range of acceptable pulse widths. Too short a pulse and the silicon will crack due to shock, while too long a pulse will allow significant energy to be diffused thermally into the wafer, leading to very deep junctions and lower solar

cell performance. The acceptable range for electron beam pulse width is about 10 ns to 200 ns for annealing ion implantation damage to the silicon crystal by liquid phase epitaxy. No successful experiments, with any technique, fall outside this range, as shown in Figure 3-1. Spire Corporation has available, from another program, an electron beam generator (the SPI-PULSE 600) with a 40-ns pulse width. It stores 20 percent of the energy of the existing pulse annealing equipment at the same charging potential in 1/20 of the volume. It was used to answer the question on the suitability of lower energy beams for implant annealing. For comparison, commercially available equipment[4] currently used for semiconductor processing has a pulse width 100-150 ns long and is adjustable, but has a maximum fluence of only 0.1 joule/cm^2 per pulse, an order of magnitude too small.

Approximately 250 pulses using implanted silicon samples for diagnostic instruments as targets were processed with the SPI-PULSE 600 facility. A typical electron energy spectrum, reduced from measurements of the diode voltage and current, is shown in Figure 3-2. The average electron energy and fluence at the sample are comparable to results on the larger facility. The implant anneal pattern on a wafer is shown in Figure 3-3.

Electrical solar cell measurements of these samples showed very low open-circuit voltages, less than 400 mV. The loss of V_{oc} is believed to be caused by point defects below the junction region in the pulse annealed ion-implanted silicon. This region is heated but not melted during pulsed processing, and rapid quenching[5] can introduce defects in the material. One solution to this problem is to use a more shallow deposition profile (reducing heating below the junction) of electron beams with a grazing angle of incidence. This profile is achieved in the larger pulse anneal facility by focusing the beam and causing it to rotate in a magnetic field. On the smaller facility, focusing the electron beam (but maintaining constant fluence at the sample) increased the open-circuit voltage V_{oc} to 480 mV. A suitable magnet was not available, but it is believed that the use of magnetic fields would increase the electrical performance of a pulse anneal to the level seen on the larger facility.

Because the electrical performance of implanted silicon samples annealed by the lower energy beam was less than the performance of samples annealed by the standard beam used to date, a second series of experiments was performed on the SPI-PULSE 6000 facility, using an aperture at the anode to reduce beam size. The experimental apparatus was similar to that shown in Figure 2-4, except that the carbon mask was placed next to the anode or used in place of the anode. The mask had circular holes with various

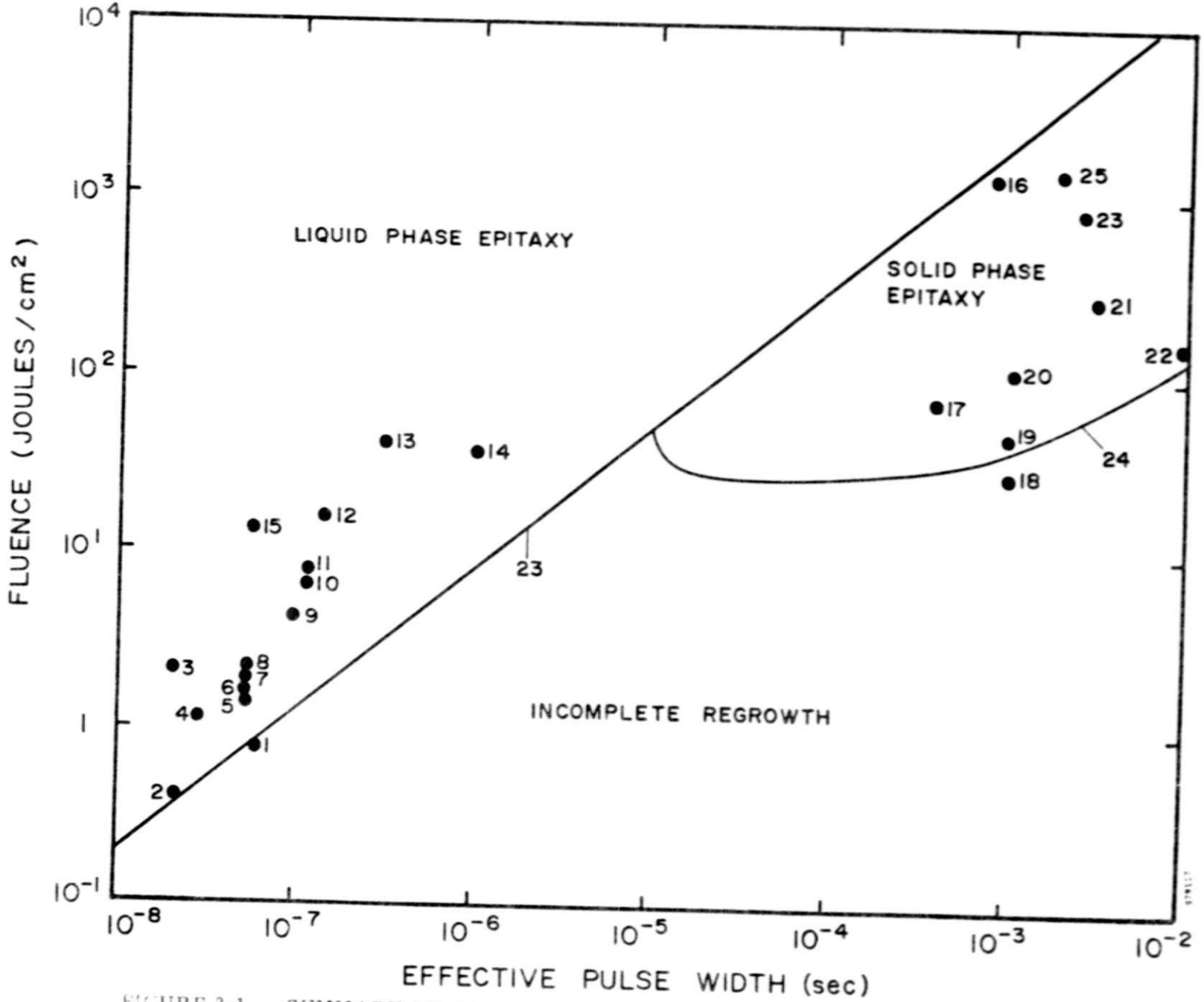


FIGURE 3-1. SUMMARY OF EXISTING EXPERIENCE ON THE USE OF PULSED ENERGY ANNEALING OF ION IMPLANTATION DAMAGE (Note: Numbers beside data points are referenced on p. 3-4.)

REFERENCES FOR DATA POINTS OF FIGURE 3-1

No.	First Author	Journal	Laser
1	Kirkpatrick	IEEE Trans. ED-24, 429 (1978)	e-beam
2	Shtyrkov	Sov. Phys. Semicond. 9, 1309 (1975)	Nd:YAG
3	Revesz	Appl. Phys. Lett. 33, 431 (1978)	Ruby
4	Narayan	J. Appl. Phys. 49, 3912 (1978)	Ruby
5	Young	Appl. Phys. Lett. 32, 139 (1978)	Ruby
6	Lysenko	Sov. Phys. Semicond. 11, 1327 (1977)	Ruby
7	Foti	J. Appl. Phys. 49, 2569 (1978)	Ruby
8	Foti	Phys. Lett. 65A, 430 (1978)	Ruby
9	Kutukova	Sov. Phys. Semicond. 10, 265 (1976)	Ruby
10	Celler	Appl. Phys. Lett. 32, 464 (1978)	Nd:YAG
11	Beri	Appl. Phys. Lett. 33, 137 (1978)	Ruby
12	Bean	Appl. Phys. Lett. 33, 227 (1978)	Nd:YAG
13	Celler	Appl. Phys. Lett. 32, 464 (1978)	CO_2
14	Kistemaker	(Unpublished) FOM-42.593, AMOLF-77/260 (Amsterdam) (1977)	Nd:YAG
15	Greenwald	(Unpublished) Spire Corp. (1978)	CO_2
16	Gat	Appl. Phys. Lett. 32, 276 (1978)	Ar
17	Gat	Appl. Phys. Lett. 33, 389 (1978)	Kr
18	Minnucci	(Unpublished) Spire Corp. (1976)	Ruby
19	Minnucci	(Unpublished) Spire Corp. (1976)	Nd:YAG
20	Kachurin	Sov. Phys. Semicond. 11, 1178 (1977)	Flash lamp
21	Antonenko	Sov. Phys. Semicond. 10, 81 (1976)	Ruby
22	Kachurin	Sov. Phys. Semicond. 10, 1128 (1976)	Ar
23	Greenwald	(Unpublished) Spire Corp. (1978)	e-beam
24	Williams	Appl. Phys. Lett. 33, 542 (1978)	Ar
25	Auston	Appl. Phys. Lett. 33, 539 (1978)	Ar

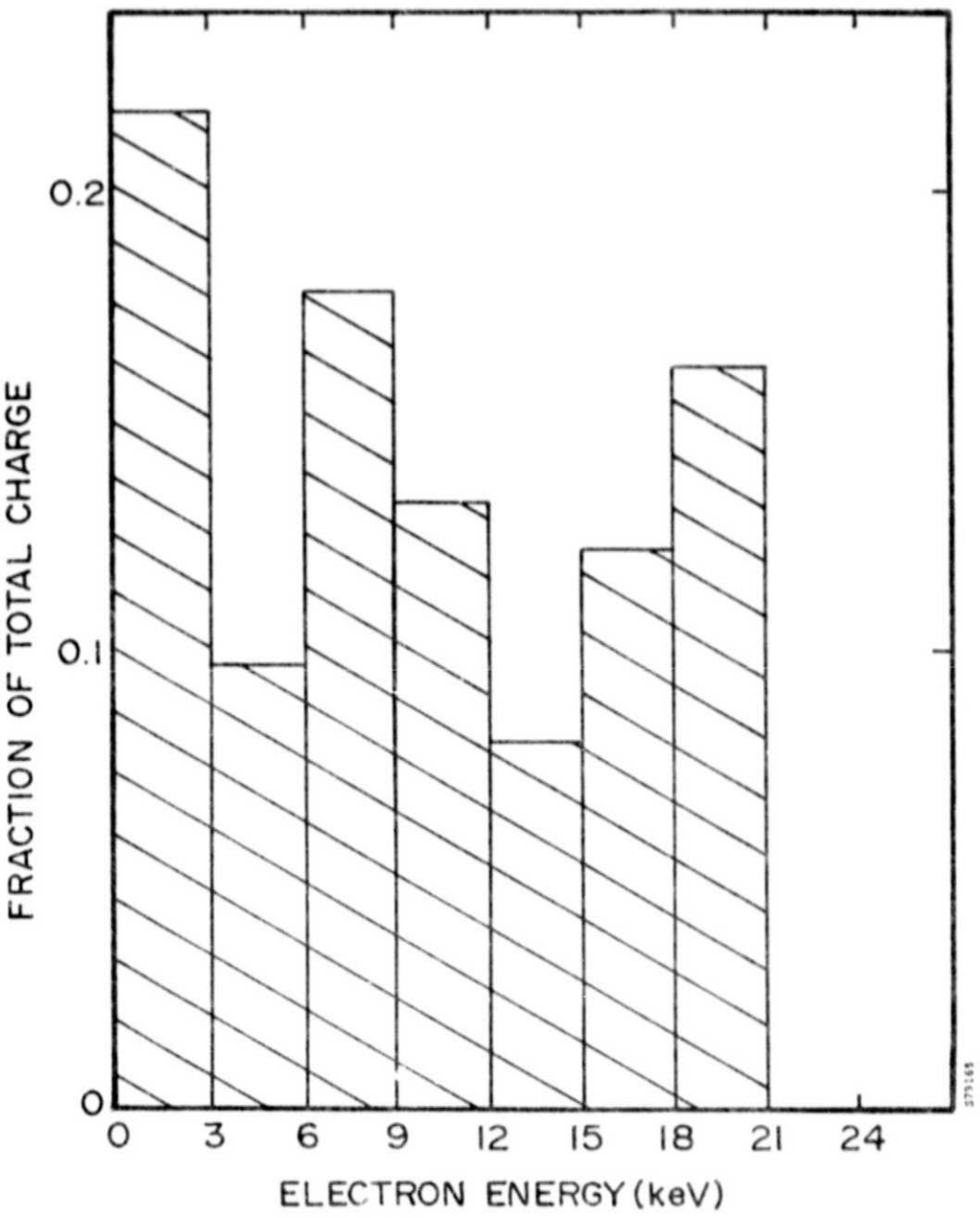


FIGURE 3-2. ELECTRON BEAM ENERGY SPECTRUM FOR SPI-PULSE 600 PULSED ELECTRON BEAMS



FIGURE 3-3. TYPICAL PULSED ELECTRON BEAM ANNEAL SIGNATURE FOR OVERLAP PULSES FOR STEP AND REPEAT OPERATION OF SPI-PULSE 600

diameters. The important physical difference in location of the mask is that the propagation of a smaller diameter, low-current beam from the anode to the sample shows less self-interaction than the larger, high-current beam and in effect resembles a small electron beam generator. Experimental results showed the lack of beam self-focusing. The electron beam fluence was too low with the standard beam in the diode. Increasing the charging voltage in the energy storage capacitor increased both the current and average electron energy in the apertured beam, which did anneal the ion-implant damage but with poor electrical results, similar to those from the smaller facility. Increasing the current density without focusing by decreasing the cathode diameter from 7.6 to 5.0 cm increased the diode impedance. The charging voltage was then adjusted to maintain approximately the same electron energy spectrum, and samples were adequately annealed with the small aperture in place. The carbon mask could not be used as an anode when the diameter of the opening greatly exceeded the cathode-anode gap.

As a result of these experiments the following conclusions were drawn with respect to the design of the pulse forming network (PFN):

- With constant fluence at the silicon wafer, and with constant electron energy spectrum, the diameter of the pulsed beam may be varied.
- There is no minimum beam diameter or total energy except as implied by the criterion of large angles of incidence of the electrons at the sample surface.
- The anode is essential for the propagation of the electron beams of interest for annealing when the current at the appropriate electron energy (10-12 keV) exceeds the space charge limiting value of approximately 5 amperes.

3.1.1 Power Supplies for Pulsed Electron Beam Processors

Power supplies for pulse processor applications must be chosen primarily on the basis of the maximum voltage required to charge the energy storage capacitor, and the maximum necessary charging current for the required repetition rate. The latter is a function of both the capacitance of the store and the pulse repetition rate. For one-of-a-kind experiments and single shot processing, Van de Graaff generators, operable up to 400 kVdc and 50 microamperes, have proven useful. Repetitive processing at intermediate rates of about 10 cm^2 of annealed surface per second requires a power supply with a 1 mA current at 300-400 kV, while final processing goals of 600 cm^2/sec may require supply currents up to 100 mA. Output currents of this magnitude place exceedingly harsh demands on all but the most carefully designed high-voltage power supplies.

Two categories of commercially available supplies will be useful for these higher current applications. Gas-insulated, multistage Crockroft-Walton high frequency (30 kHz) driven units can supply the 1-2 mA currents required for intermediate processing applications of up to 50 cm^2/sec. The inherent compactness of the high-voltage multiplier section in the Crockroft-Walton supply allows its installation directly inside the enclosure of large PFN's like the SPI-PULSE 6000, which are generally operated in a high-pressure, insulating gas environment. The need for high-voltage supply cables and feedthrough bushings from supply to energy store is thus eliminated. In addition, the ability to control the supply output voltage with a small control voltage makes such supplies ideal for programmed repetitive charging cycles. A

PFN charging system for a 10 cm^2/sec pulse processor for implant annealing which incorporates a commercially available supply is summarized in Figure 3-4.

A single multistage Crockroft-Walton power supply cannot provide the 100-mA charging currents necessary for the final processing goal of 600 cm^2/sec. For this more demanding application, a 60-Hz transformer-rectifier supply appears necessary. This type of supply must generally be mounted externally and connected to the PFN with a high-voltage cable because of its large size. There appears to be little advantage to using gas-insulated high frequency supplies when external mounting is required. Many traditionally designed and well tested oil-immersed power supplies are commercially available at costs lower than Crockroft-Walton supplies rated at the same voltage and current. The most critical component of external power supplies is in fact the connecting cable and feedthrough bushing to the high-pressure capacitor. The highest voltage levels of 400 kVdc used in pulse annealing applications appears to be within the limits of state-of-the-art technology in this area.

The relative costs of the supplies discussed in this section are summarized in Table 3-1.

TABLE 3-1. COMPARATIVE SPECIFICATIONS AND COSTS FOR POWER SUPPLIES FOR PULSE PROCESSOR APPLICATIONS

Power Supply	Representative Commercial Unit	Voltage (Current)	Annealing Rate	Approx. Cost
High Frequency Crockroft-Walton Multiplier	Deltaray S-400	400 kV (1 mA)	10 cm^2/sec	$10,000
Transformer-Rectifier	Hippotronics 2300	300 kV (10 mA)	100 cm^2/sec	$9,000
Transformer-Rectifier	Universal Voltronics BAL-300	300 kV (100 mA)	600 cm^2/sec	$20,000
Transformer-Rectifier	Universal Voltronics	450 kV (80 mA)	600 cm^2/sec	$50,000

3.1.2 Pulse Forming Network

Experimental work to date at Spire has demonstrated the usefulness of existing coaxial-charge-store pulse forming networks (PFN's) for PEBA applications. In particular, the incorporation of a DC charged, solid dielectric energy store into the PFN allows control of beam energy at a level of precision not generally obtainable with dynamically charged gas or liquid dielectric energy stores. Such precision is essential for the reproducibility of the pulse processing of ion-implanted silicon.

The major drawback of solid dielectrics has generally been their lack of self-reparability in the event of high-voltage breakdown of the insulator. Nevertheless, capacitor prototypes developed at Spire using advanced manufacturing techniques and optimized dielectric materials have not yet experienced volume puncture after more than 10^3 shots at the designed charging voltage of 400 kV.

Operation of such energy storage capacitors at lower voltages near 100 kV will greatly increase the projected lifetime. We estimate a minimum of 10^7 - 10^8 shots, based on available lifetime data from pulsed capacitor manufacturers. Experiments to date indicate that successful anneals at these lower voltages should be possible.

Another source considered possible for use as a PFN energy store involves the use of several commercial, low-inductance capacitors available at rated voltages up to 100 kV. The chief advantage of lower system cost is offset by the increased system inductance, which leads to longer risetime of the electron beam pulse. Total energy store charging voltage will generally be lower, in the 50-100 kV range, so that capacitor lifetime can be enhanced by major voltage derating. Preliminary estimates, based on a system using eight rectangular 100-kV, 20-nanohenry, 0.3-microfarad capacitors, indicate that risetimes on the order of two or three times longer than those achievable with existing coaxial PFN's should be possible. It is not yet known whether the increased risetimes will influence the pulse annealing mechanism.

3.1.3 High Voltage Switching

Large-scale pulse annealing processors will require reliable, long-lifetime, high-voltage switches for activation of the electron beam pulse. This relatively underdeveloped area of technology will be an extremely critical one in any final processor design for production applications.

Continuous-duty switching problems occur because electrode materials deteriorate in time with the necessary current levels. Degradation of the insulating medium, usually a gas between the switch electrodes, can also occur. Various investigators elsewhere have identified important high-voltage pulsed switch parameters, but design criteria have by no means been optimized.

Switch experiments planned on existing Spire high-repetition-rate pulser facilities are aimed at selecting the best switch design for our specific pulseforming network and pulse annealing applications.

3.2 SCANNING DC ELECTRON BEAM ANNEALING

As part of the determination of the manufacturing feasibility of pulse annealing, DC, or continuous, electron beam scanning has been assessed as an alternative method of directed annealing. Calculations were performed to evaluate the feasibility of annealing large silicon sheets on a suitable platen or carrier. Input data for the calculation was as follows:

Material:	Polycrystalline sheet silicon
Thickness:	0.38 mm (0.015 inch)
Size:	20 x 20 cm
Transfer rate:	30 cm/sec
Cassette:	Silicon carbide or equivalent
Electron beam:	20 cm long x 0.5 to 50 cm wide

This calculation assumes that the final temperature is 1412^{o}C (the melting point for silicon), but none of the material is melted. It was concluded that, on the time scales of interest, the temperature profile throughout the depth of the material is nearly uniform and the flow of heat in the direction of motion is small. The calculation of heat input (average heat capacity x total mass x temperature rise) is accurate enough for initial design parameters. The transfer of heat by radiation to the surrounding space or conduction to the wafer cassette is small but nonnegligible compared to the thermal input.

Approximate Calculations

The average heat capacity from 298^{o}K to 1685^{o}K for crystalline silicon, based upon the integration of the equation for heat capacity given by Runyan, is 0.916 joule/g^{o}C.[6]

The sheet is 380 micrometers (0.015 inch) thick, and its mass per unit area is 8.88 g/cm^2.

The fluence required to reach melt temperature (neglecting heat flow) is 112.8 J/cm^2.

The total beam power required at 600 cm^2/sec is approximately 68 kW.

One-Dimensional Solution to Heat Flow in a Moving Slab

The silicon slab is very thin compared to its length or width or distance traveled in one second. For an approximate pulse width of 15 msec (equivalent to the time that any point on the surface is irradiated by the electron beam), the characteristic depth to which heat is transported by thermal diffusion for a semi-infinite slab would be:

$$x \sim (4Kt)^{1/2} = (4 \times 0.224\ cm^2/sec \times 0.015\ sec)^{1/2} = 0.116\ cm \qquad (1)$$

This is approximately three times the width of the slab, justifying the assumption of a uniform temperature profile throughout the thickness of the slab.

To compute the flow of heat along the slab, on neglecting edge effects since there is no variation in depth $\hat{z}$ or thickness $\hat{y}$, the problem is one-dimensional in the direction of motion of the slab, $\hat{x}$. For a thin, infinitely long rod with a perimeter p and cross-sectional area w — moving in the direction $\hat{x}$ at a constant velocity u, with the point at $x = 0$ held at a fixed temperature T_1 — the temperature profile is given by Carlsaw and Jaeger:

(2)

$K = \kappa/\rho C$ = thermal diffusivity
κ = thermal conductivity
ρ = density
C = heat capacity
$\nu = Hp/\rho Cw$
p = perimeter
w = cross-sectional area
H = surface conductance

The rate of heat loss from the surface of the rod is assumed to be proportional to $H(T-T_o)$, where T_o is the temperature of the surroundings and T varies with x. The units of H are in watts/cm^2•deg. For this problem, the rod has one dimension equal to the thickness of the slab (0.015 inch) while the other dimension $\Delta \to 0$. Therefore:

$$w = (0.5p - d)\, d$$

$$p = 2(d + \Delta)$$

or

$$\nu = H\Delta/\rho c w = H\Delta/\rho c \Delta d = H/\rho C d$$

Typical values for H for aluminum-aluminum contacts in vacuum, for parts with a fine surface finish but not "optically flat", is approximately 30 BTU/hr-ft^2-^{o}F at 10 PSI pressure between the two surfaces. On assuming this behavior is similar for both rough-cut silicon wafers and ribbon with a silicon carbide "flat" holder and also on assuming a pressure of 0.1215 PSI and $H \propto P^{2/3}$, then $H \sim 9.0 \times 10^{-4}$ W/cm^2 - ^{o}C. (Note: Data is taken from the Handbook of Heat Transfer.) Another approximation would assume purely radiative heat transfer as T^4 with a maximum value of 45.7 W/cm^2, which, divided by the temperature, gives $H \sim 0.027$ W/cm^2 - ^{o}C. The radiation treatment does not follow from the linear heat loss rate with temperature used to develop Equation (2), which overestimates the cooling.

The value of ν can now be estimated at between 0.011 and 0.33 sec^{-1}. The value of $K\nu$ is at most 0.074 cm^2/sec compared to 900 cm^2/sec^2 for u^2. Therefore, Equation (2) can be simplified:

$$\frac{u - (u^2 + 4K\nu)^{1/2}}{2K} \; x \cong -\nu x/u \qquad (3)$$

$$T \cong T_1 \exp(-\nu x/u)$$

where:

$$0.011 < \nu/u < -3.7 \times 10^{-4}$$

The physical interpretation of the results is that the distance for the temperature of the slab to drop from its maximum of 1685^{o}K to room temperature is greater than 90 cm. Cooling by heat transfer along the slab is very small compared to the heat loss through the upper or lower surface.

Fast Pulse Heating

The assumption of a 0.015-sec pulse width was based on a sheet electron beam width of 4.5 mm (30 cm/sec x 15 msec). The electron beam could be focused to about 0.5 mm for a pulse width of 1.66 msec. The effect of this shorter pulse will be computed assuming negligible heat transfer along the slab in the $\hat{x}$ direction. The problem is again one-dimensional (heating a semi-infinite slab) in the $\hat{z}$ direction. The surface temperature is given by W.R. Neal, Spire Corporation, in Report No. TR-78-02:

$$T \cong \dot{F}\, x(t)/\sqrt{\pi \kappa}$$

where κ is the thermal conductivity and x is given by Equation (1). Here x = 0.0386 cm, about equal to the substrate thickness, and the fluence F to reach melt is about 51 joules/cm^2. The reduction of a factor of 2 for part (1) is due to not heating the entire substrate uniformly throughout its thickness. Recommended beam parameters form this calculation are:

Fluence:	51 joules/cm^2
Energy:	20 keV
Length:	20 cm
Width:	0.5 mm
Current:	1.5 A/cm^2

Some relaxation of the beam current density may be possible by expanding the width of the line beam to 10 mm; however, 45-mm electron beam line widths would not allow sufficient current density for the required temperature rise.

The important distinction of annealing by scanned DC electron beams as contrasted to pulsed electron beam annealing is the physical mechanism responsible for lattice regrowth. Scanned DC electron beam power densities are limited to temperature increases below the melting point because the entire silicon sheet is uniformly heated and cannot be allowed to melt. Because there would not be a thermal gradient under these heating conditions, any solid phase regrowth occurs extremely rapidly at 1100-1400°C, and polycrystallite formation can be expected to occur in amorphous, implanted layers as the transition occurs to the crystalline phase. In addition, rapid thermal quenching of the silicon material from 1100-1400°C to 25°C will induce recombination centers, decrease minority-carrier lifetime, and lower the solar cell performance.

Economic disadvantages of bulk wafer heating are also inherent for DC scanned electron beam heating. The primary consequence of high-temperature substrate heating is the increased demands on material handling equipment. For example, silicon carbide wafer platens would be required to prevent nonintentional doping of the silicon substrate, and molybdenum or tantalum conveyors would be required for high temperature stability.

3.3 BELT FURNACE HARDWARE

As described in Section 2.3, an anneal test matrix was designed and carried out to develop a more cost-effective furnace annealing cycle for solar cell manufacturing. Belt furnaces with in-line material transport are now commonly used in the thick-film hybrid circuit industry for sintering noble metals in hydrogen/nitrogen atmospheres. Experiments are being conducted to determine if:

1. Solar cell performance can be maintained in a belt furnace.
2. The use of cracked ammonia or hydrogen atmosphere in the belt furnace can eliminate the need for HF etching to remove oxides normally found in nitrogen atmosphere annealing.

Cost estimates for belt furnaces with throughputs of 50 and 125 cm^2/sec are being prepared. The furnace for implant annealing is designed to reproduce closely the 850°C-15 minute plus 550°C-60 minute cycle now being used at Spire for tube furnace annealing. An outline drawing of a 125 cm^2/sec belt furnace is shown in Figure 3-4. In each furnace, 4.3m is allowed for entrance and exit material-handling to eliminate oxygen and water vapor from the hot zone and to allow stacking of the silicon carbide, duramic, or other high-temperature carrier platens. As shown in Figure 3-4, two transport speeds are required. One transport system operates at 12 cm/sec for the initial transfer of the wafer carriers and for stacking the carriers into modules before entrance into the furnace hot zone. The modules, with dimensions of 20 x 20 x 20 cm, will contain 64 carriers each with a capacity of 400 cm^2 of silicon. Stacking the carriers into such modules is required to minimize the overall length of the belt furnace. The second transport system within the hot zone of the furnace operates at 0.2 cm/sec for a total time of 75 minutes. The heat load on the furnace elements will be 48 lb/ft, typical of exiting furnace conveyors. Major system parameters for a 125 cm^2/sec belt furnace are outlined in Table 3-2.

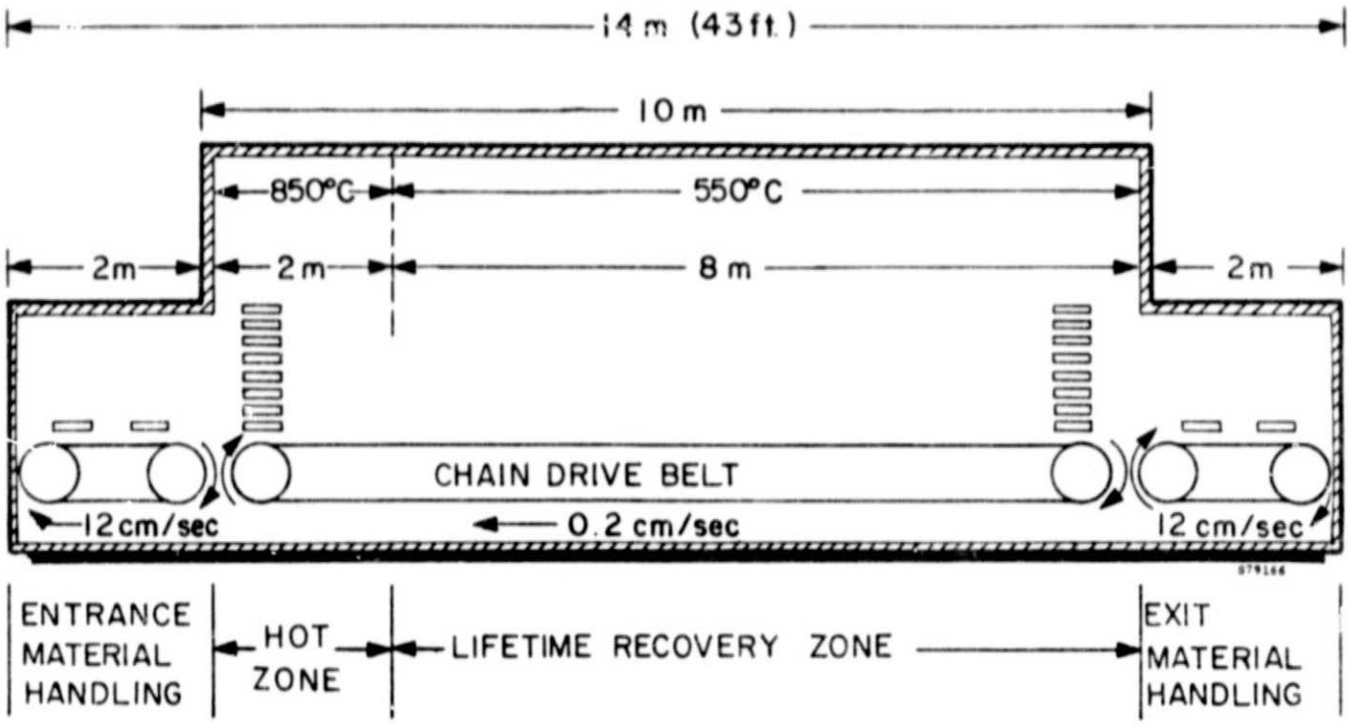


FIGURE 3-4. SCHEMATIC FOR 125 cm^2/sec BELT FURNACE FOR IMPLANT ANNEALING

TABLE 3-2. FUNCTIONAL REQUIREMENTS FOR 125 cm^2/sec BELT FURNACE FOR IMPLANT ANNEALING

Item	Specification
Belt width:	63 cm
Belt speed:	0.2 cm/sec (loading)
Silicon carrier size:	20 x 20 x 0.3 cm thick
Module size:	20 x 20 x 20 cm (64 carriers/module)
Carrier material:	Silicon carbide, duramic, or equivalent
Throughput:	125 cm^2/sec
Heat loading:	24 kg/linear meter

SECTION 4
SUMMARY

This report has described the fifth quarter results of a program whose purpose is to develop ion implantation and associated pulse processing for long-range automated production of solar cells. Significant accomplishments during this reporting period include:

1. Selection of a manufacturing process sequence which utilizes ion implantation for both junction and back surface field (BSF) layers in 10-ohm-cm Czochralski silicon material. The process sequence also incorporates pulse processors for annealing of the ion implantation damage and sintering of contact materials.

2. Identification of a more cost-effective furnace annealing cycle for simultaneous phosphorus and boron implants for junction and BSF introduction. This cycle requires only 75 minutes compared to 265 minutes for the earlier, performance-optimized anneal cycle.

3. Demonstration of a step and repeat operational mode for the pulsed electron beam annealing of areas up to 20 x 20 cm on sheet silicon materials.

4. Development of the required beam parameters for the generation of reproducible and uniform 7.6-cm diameter pulsed electron beams. These beam parameters have been used to anneal successfully both boron and phosphorus implants in 7.6-cm wafers with a single pulse.

SECTION 5
RECOMMENDATIONS

Satisfactory pulse processors for annealing ion implantation damage in silicon should be identified with throughput rates between 50 and 500 cm^2/sec. As a part of this development, requirements should be identified for long-term, high repetition rate operation.

Further machine and process-sequence development should now be directed toward the doping method for p+ layers. This development should include SAMICS analysis of non-mass-analyzed aluminum ion sources and charged particle deposition. Selection of hardware should be made so that the hardware can be integrated in a pulse processor. The proposed process sequence would include:

1. p+ introduction
2. pulse anneal
3. ion implantation for junction
4. pulse anneal

A junction processor for such a sequence should then be designed to achieve economy of scale for throughputs between 50 and 500 cm^2/sec.

SECTION 6
NEW TECHNOLOGY

No new technology has been developed to completion during this quarter.

SECTION 7
PROGRAM SCHEDULE

The program schedule is given in Figure 7-1. Progress remains on schedule with most of the tasks completed by the original milestones. No serious problems have been encountered during this reporting period. Efforts have been redirected by JPL to emphasize cost-effective furnace anneal optimization and to postpone determination of the optimized throughput for integrated ion implanter/pulse processor hardware. Contract efforts are now concentrated on processing and delivery of (500) pulse annealed solar cells.

FIGURE 7-1. PROGRAM SCHEDULE

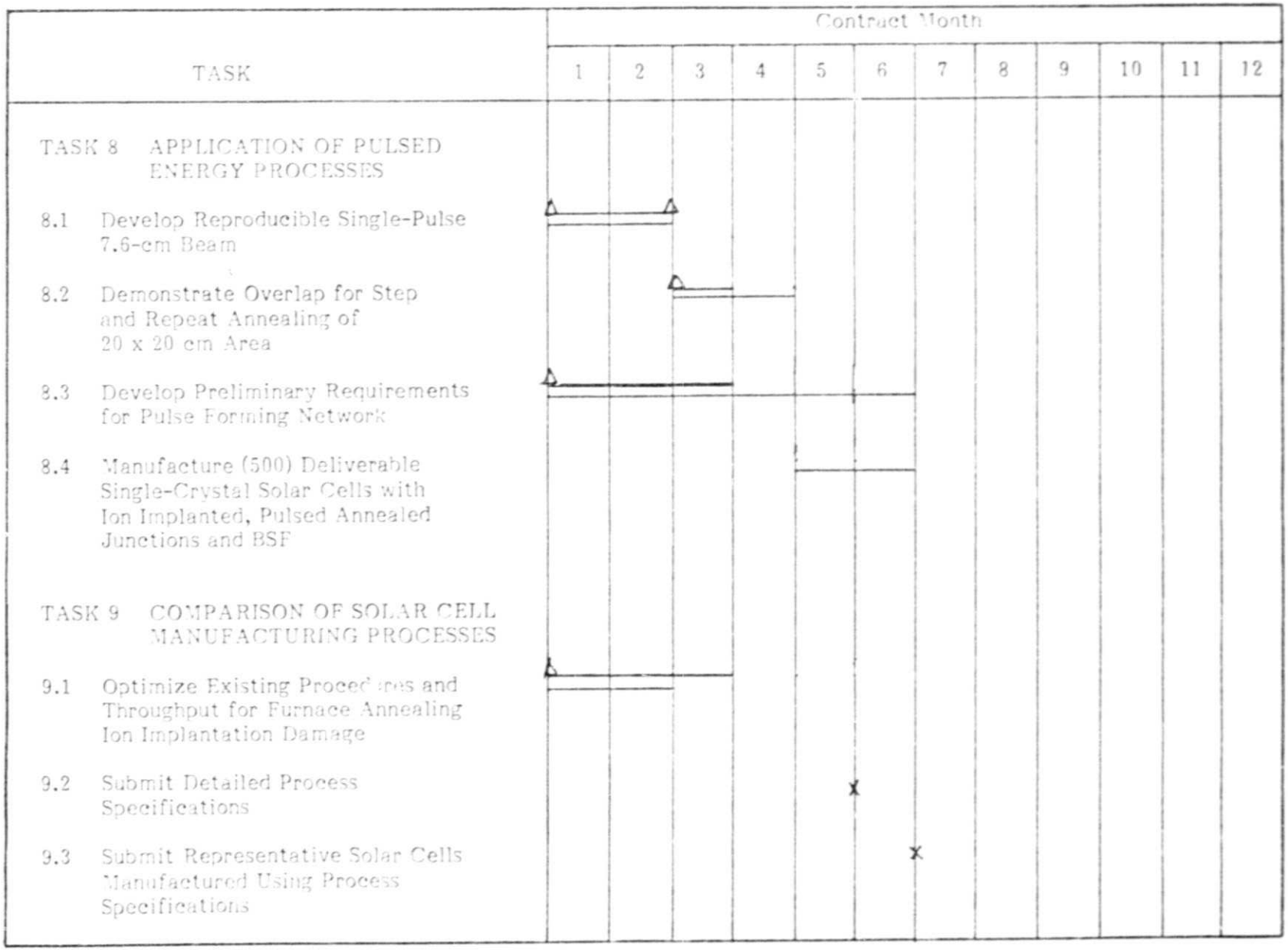
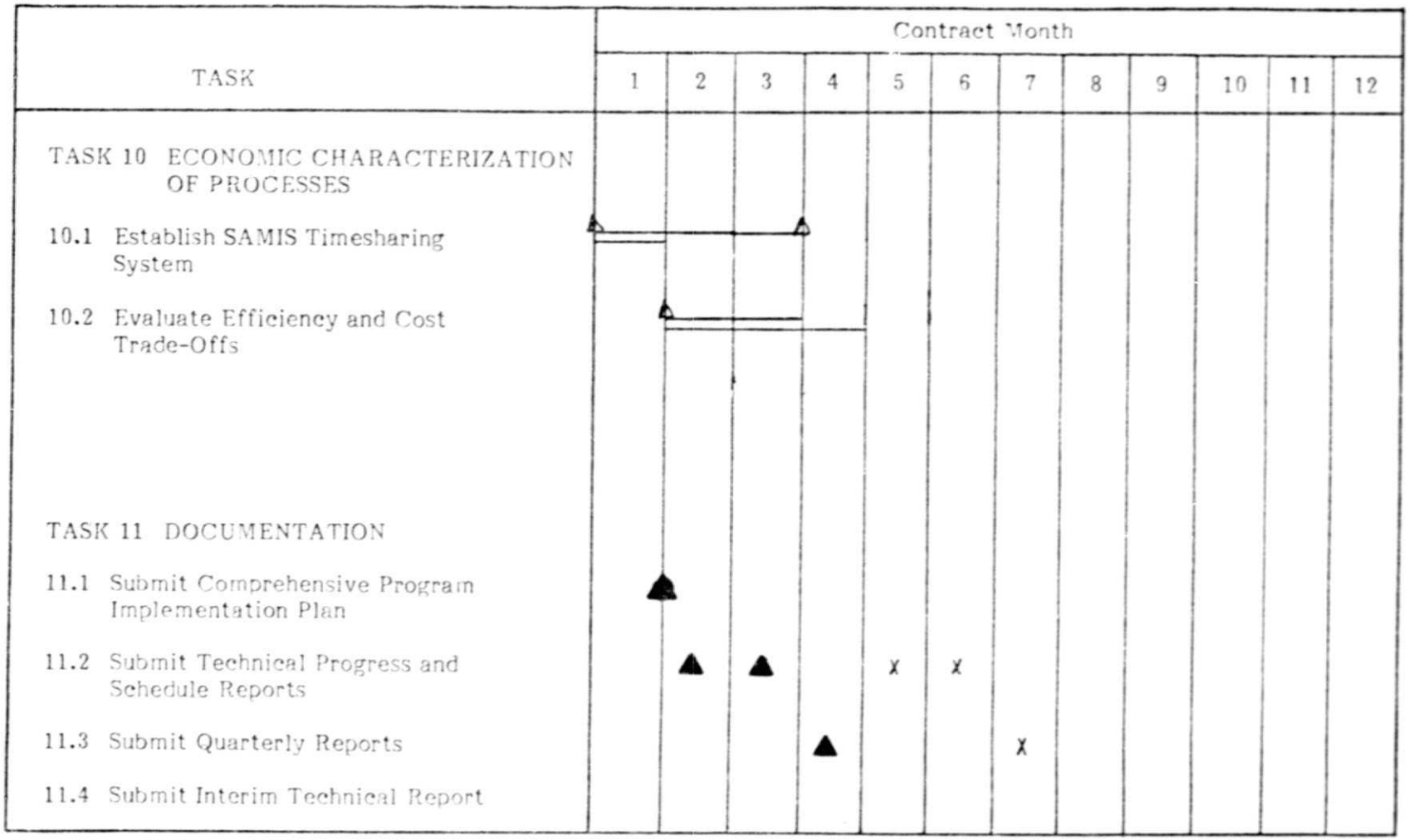


FIGURE 7-1. PROGRAM SCHEDULE (Concluded)



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